A Simplified 3-D NLM-Based SVPWM Technique with Voltage Balancing Capability for 3LNPC Cascaded Multilevel Converter

Abstract— The nearest level modulation (NLM)-based space vector pulse width modulation (SVPWM) algorithms have attracted a great deal of interest since they can provide various degrees of freedom, i.e., optimized switching sequences and adjustable duty cycles. This paper proposes a simplified three-dimensional (3-D) NLM-based SVPWM algorithm in a 3-D coordinate system. Compared with the generalized two-dimension (2-D) NLM-Based SVPWM schemes, the proposed method not only provides identical degrees of freedom to optimize switching patterns and obtain adjustable duty cycles, but also presents better digital implementation and lower hardware occupancy to achieve the real-time PWM generation. In addition, based on the NLM-based principle, a method of addressing the issue of unbalanced voltages in a three-phase 3-Level Neutral Point Clamped Cascaded Multilevel Converter (3LNPC-CMC) is introduced. The presented method possesses the optimized voltage balancing capacity and equalizes the unbalanced inner-cell and mutual-cell voltages in the 3LNPC-CMC with minimum number switching transition. Finally, the whole proposed process is verified by simulation and experimental results.

***Index Terms*— 3-D SVPWM, simplified digital implementation, degrees of freedom, optimized voltage balancing capability, multilevel converters, 3LNPC-CMC.**

I. INTRODUCTION

Multilevel converters have the increasing tendency in the application of high-power high-voltage occasions due to the reduced stress on switching devices and the improved harmonic performance [1]-[3]. During the past decades, various multilevel topologies have been evolved and divided into several kinds, mainly including diode-clamped, flying capacitor-clamped, cascaded H-bridge and modular multilevel converters, etc [4]-[7]. Along with the growth of the multilevel topologies, a lot of pulse width modulation (PWM) techniques have been developed [8]-[10]. Most of them can be classified into three kinds: 1) Carrier-based PWM method [11]-[12]; 2) Nearest-level modulation (NLM) method [13]-[14]; 3) Space vector pulse width modulation (SVPWM) method [15]-[16]. Among these, the SVPWM method became popular since it can achieve the better utilization of dc capacitor voltages, more flexibility in the switching pattern choice and the reduced switching frequency of devices.

Conventional SVPWM methods [17]-[21] for n-level converters may involve several steps: 1) detecting the nearest three vectors (NTVs) to synthesize the reference vector by identifying the sectors and the modulation triangles; 2) calculating the dwelling duty cycles of NTVs; 3) listing all space vectors with lookup table modules; 4) comparing the duty cycles with triangular carrier to generate trigger signals. Although the SVPWM schemes have many advantages, it is still difficult for application in higher level converters. For the conventional SVPWM schemes, there are $6(n\text{-}1)^2$ modulation triangles and n^3 space vectors as the level increases. Thus, they are not only complex and difficult to identify the sectors and choose redundant space vectors, but also undermine the flexibility of achieving more potential performance.

Hence, some simple three-phase SVPWM methods are proposed. In [22]-[25], SVPWM schemes that operate on the 60° or 45° or other 2-D coordinate system can significantly reduce computational complexity as look-up tables are not required. However, with the level numbers of converter increasing, the computational complexity also increases. In addition, they seem not exploiting the ability to improve the performance of multilevel converters.

Based on 2-D SVPWM schemes, several 3-D SVPWM algorithms have been proposed[26]-[28], in which three axes are oriented at 90° to each other to form a cubic space. It grows as a subcube with increasing in level numbers of the converters. They are independent of the number of levels and useful in systems with or without neutral and unbalanced loads. However, they require to detect and switch four space vectors. Also they still do not conclude the effective strategies to obtain some degrees of freedom to improve the potential performance of converters.

Aiming at further obtaining given performance, some simplified SVPWM schemes [29]-[30] extra apply the minimum energy property of multiple dc-link capacitors to balance the dc capacitors and [31] offer a method to reduce the common-mode voltage. All of them acquire corresponding effectiveness. But meanwhile incorporation of these process into the algorithms make the digital implementation more complex. Based on [29]-[30], some newest SVPWM algorithm in [31]-[32] with some controlled factors, including optimized switching sequences and adjustable duty cycles, to improve the properties of multilevel converters. Moreover, they are also independent of level numbers and even had the actual applications. Whereas, for these schemes, the detection of

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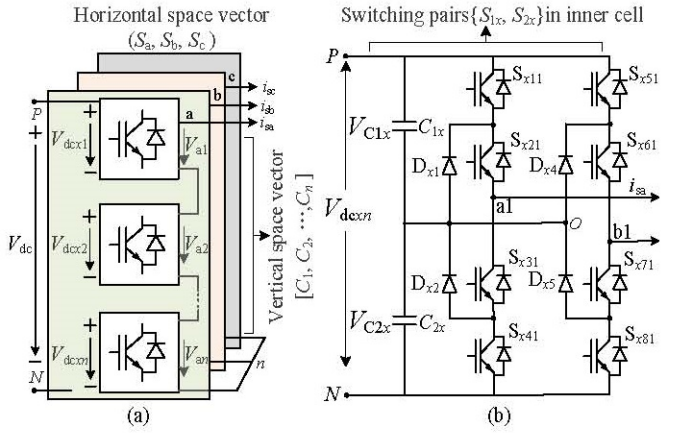

Fig.1. The simplified topology of three-phase 3LNPC cascaded multilevel topology: (a) Three-phase cascaded multilevel converter; (b) 3-Level Neutral-point-clamped converter of a single cell.

vector is realized by determining a set of nested hexagons. This will require iterative calculations.

The amount of calculations required are compared to prior methods[29]-[32]. Other new NLM-based SVPWM algorithms have been studied in [33]-[35]. They attempt to further reduce the complex arithmetical calculations and provide the flexibility for improving the potential performance of the converters based on the NLM principle. Specially, the sequencematrices are applied to obtain gate pulses for any level converters. The major deficiency of these scheme is that the required matrices and the trigonometric calculations need to be pre-stored in the memory modules. Hence the real-time calculations cannot be guaranteed. Also the required matrices are hard to generate the discontinuous operational mode and balance the unbalanced voltages. It needs to be reminded that these existing NLM-based SVPWM schemes still involve complex arithmetic calculations in the whole implementation.

Therefore, on the basis of [33]-[34]. The focus of this paper is to present a simpler and real-time 3-D SVPWM technique with identical degrees of freedom compared with 2-D well-known SVPWM. Based on NLM-based characteristic, a optimized voltage balancing algorithm is introduced to balance the inner-cell and mutual-cell unbalanced voltages in 3LNPC-CMC.

The proposed SVPWM algorithm has the following salient points:

1) Instead of calculating three space vectors in the generalized algorithms, merely one of three horizontal space vectors need to be detected in the proposed one.

2) It is independent of level numbers and suitable for various multilevel converters, like diode-clamped, flying capacitor -clamped, cascaded H-bridge and modular multilevel converter, etc.

3) The whole modulation process is real-time and merely some simple arithmetic operations need to be calculated.

4) Redundant switching sequences and different modulation modes can be flexibly generated and chosen.

5) Due to the NLM-based characteristic, a optimized voltage balancing algorithm can be introduced to address the issue of unbalanced voltages in 3LNPC-CMC with the minimum number of switching transition.

The rest of the paper is organized as follows:

Section II-A establishes the 3-D coordinate system; Section II-B introduces an alternative method in the 3-D coordinate system to detect the nearest space vector among three space vectors enclosed the modulation triangle and generate the controlled m factor; Section II-C to D deduce the potential relationship in achieving the optimized switching sequences and the adjustable duty cycles between the proposed 3-D coordinate system and the NLM-based 2-D coordinate system in [33]-[34], then demonstrate the simpler implementation of the proposed 3-D SVPWM technique. Section III defines the concept of vertical space vectors and introduces a optimized voltage balancing algorithm for 3LNPC-CMC. Section IV illustrates some simulation and experimental results as well as the comprehensive comparison with the existing SVPWM methods in different aspects. Section V concludes the paper.

II. The Proposed 3-D SVPWM Technique

A. Forming the 3-D space coordinate system

Fig.1(a) shows the simplified circuit of three-phase 3LNPC cascaded multilevel converter. Fig.1(b) shows a 3-level neutral-point-clamped converter which can achieve five-level output. Obviously, the cascaded converter consists of cascaded 3LNPC and has superiority advantages of higher voltage endurance capability and more modularity compared with 2-level cascaded topology in [31].

In Fig.1, i_{sa}, i_{sb} and i_{sc} are the AC output currents; C_{1x} to C_{2x} are two capacitors in inner cell; V_{C1x} to V_{C2x} are their voltages. V_{dcx1} to V_{dcxn} present the dc-link voltages in every cell for phase x (x=a, b, c) ; V_{dc} is the total dc-link voltage; V_{a1} to V_{an} are the port voltages of phase a. In order to facilitate the analysis, the five-level system is applied.

Normalizing V_{dc} as 4, the generalized five-level space-vector diagram is depicted in Fig.2(a). Where, ①-⑥ are the regions; "O" is the origin of space-vector diagram and (*,*,*) means horizontal space vector. The normalized instantaneous reference space vector in Fig.2(a) can be mapped into m, n and p coordinates, presented as $V_{\mathbf{m}}$, $V_{\mathbf{n}}$ and $V_{\mathbf{p}}$ to form a 3-D space (Fig.2(b)) using the following where $V_{\mathbf{a}}$, $V_{\mathbf{b}}$ and $V_{\mathbf{c}}$ are normalized instantaneous phase voltages.

$$\begin{cases} V_{\mathrm{m}} = V_{\mathrm{a}} - V_{\mathrm{b}} \\ V_{\mathrm{n}} = V_{\mathrm{b}} - V_{\mathrm{c}} \\ V_{\mathrm{p}} = V_{\mathrm{c}} - V_{\mathrm{a}} \end{cases} \tag{1}$$

Then the reference space vector $V_{\mathbf{ref2}}$ in Fig.2(b) is

$$V_{\mathbf{ref2}} = (n-1)[V_{\mathrm{m}} \;\; V_{\mathrm{n}} \;\; V_{\mathrm{p}}]^T = (n-1)(m \cdot \frac{3}{2} V_{\mathrm{dc}} \cdot e^{j\theta}) \tag{2}$$

where, m is the modulation index; θ is the angle of $V_{\mathbf{m}}$; n presents level numbers of multilevel converters.

According to (1), there are 61 constructive horizontal space vectors in Fig.2(b) and each vector can be transformed to several redundant horizontal space vectors in Fig.2(a). Given that the reference vector is synthesized in triangle T_1 (Fig.2(a)), visibly Q_{11} is the nearest vertex closet to the origin "O" among Q_{11}, Q_{12} and Q_{13}. And vertex Q_{11} has three redundant horizontal vectors , like (2,2,0), (3,3,1) and (4,4,2). Furthermore, (2,2,0) is defined as the bottom horizontal space vector (generally the bottom horizontal one is defined as (S_a, S_b, S_c)), (3,3,1) as the

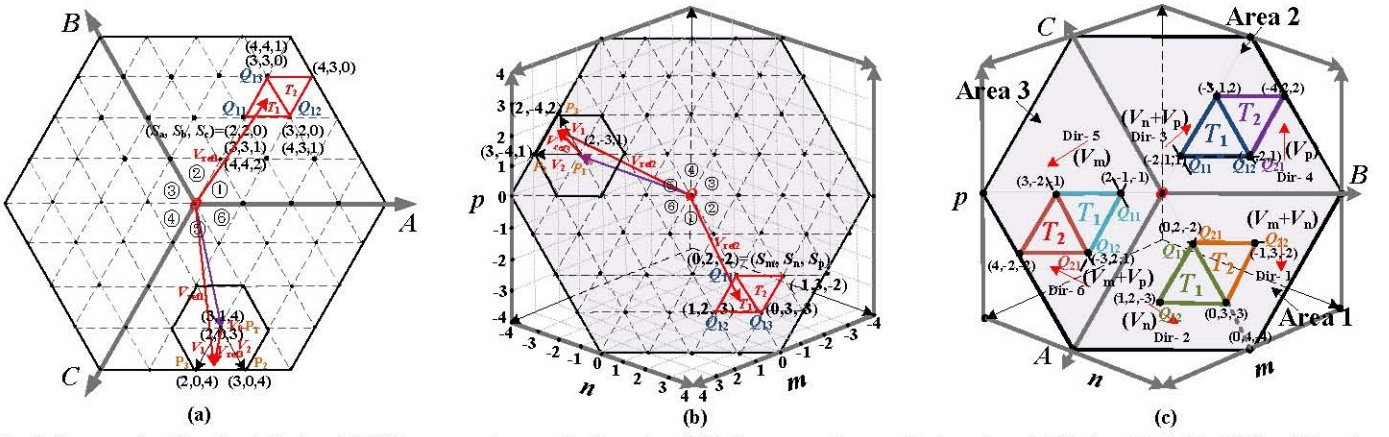

Fig. 2. Space-vector Coordinate System:(a) 2-D space-vector coordinate system;(b) 3-D space-vector coordinate system. (c) Vertex detected by (3) for different locations of the reference vector.

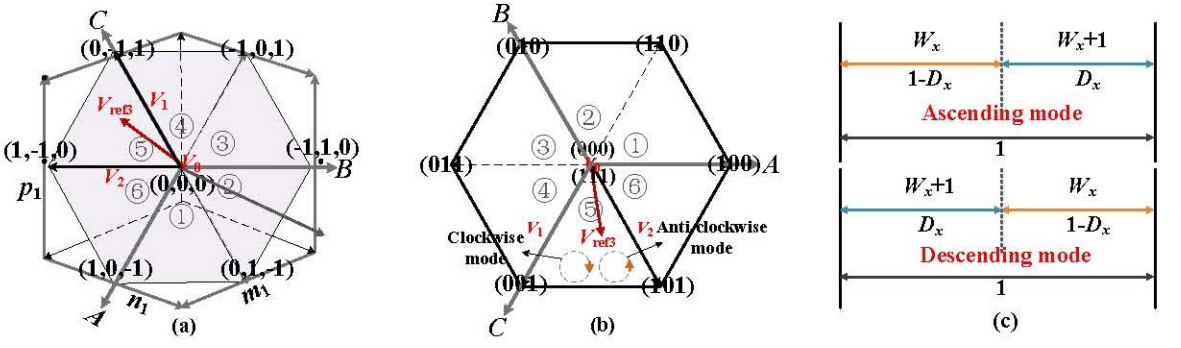

Fig. 3. Two-level diagram. (a) Two-level space vector diagram in 3-D SVPWM, (b) Two-level space-vector diagram in 2-D SVPWM, (c) Switching sequences for the ascending and descending modes in NLM.

second horizontal space vector and (4,4,2) as the top horizontal space vector (generally the second horizontal space vector and the top horizontal space vector are both defined as (S_{a1}, S_{b1}, S_{c1})). In the 3-D coordinate system, these redundant horizontal space vectors have the same constructive representation based on (1),i.e. (0,2,-2)= (2-2, 2-0, 0-2)=(3-3, 3-1,1-3)= (4-4, 4-2, 2-4). Also it is generally named as (S_m, S_n, S_p). Hence, $S_m=S_a-S_b=S_{a1}-S_{b1}$, $S_n=S_b-S_c=S_{b1}-S_{c1}$, $S_p=S_c-S_a=S_{c1}-S_{a1}$. Thus S_a, S_b, S_c and S_{a1}, S_{b1} and S_{c1} indicate the voltage level of phase a, phase b and phase c.

B. Detecting the nearest space vector

As shown in Fig.2(c), let (V_m+V_n) and (V_n) in "Area 1", (V_n+V_p) and (V_p) in "Area 2" and (V_m+V_p) and (V_m) in "Area 3" be the lines which have the increasing values in the direction of the arrows (like Dir-1 to Dir- 6). Hence, they will be notably integers when they pass through the vertices of the modulation triangles. So the nearest vertex can be easily obtained.

For example, when V_{ref2} is synthesized in triangle T_1 in Area 1, it is obvious (S_m, S_n, S_p)= (0,2,-2), so $S_n \geq 0$ and $S_p \leq 0$. It is of interest to find that the integers of (V_m+V_n) and (V_n) are equal to S_a and S_b when they pass through the vertices, i.e (S_m+S_n)= 0+2=2 and (S_n) =2. Moreover, since three-phase equilibrium, $S_m+S_n+S_p=0+2-2=0$ is obtained and thus the vertex Q_{11} = (2,2,0) is detected, which accords with the bottom space vector (2,2,0) in T_1 in Fig.2(a).

Similar analysis can be applied to other areas, hence (S_a, S_b, S_c) is generally obtained as

$$(S_a,S_b,S_c)=\begin{cases}(\text{int}(V_m+V_n),\text{int}(V_n),0) & (V_n\geq 0\,\&\,V_p\leq 0)\\ (0,\text{int}(V_n+V_p),\text{int}(V_p)) & (V_m\leq 0\,\&\,V_p\geq 0)\\ (\text{int}(V_m),0,\text{int}(V_m+V_p)) & (V_m\geq 0\,\&\,V_n\leq 0)\end{cases} \quad (3)$$

where, int(.) stands for the integer parts of the variables; Sign"&" means two required conditions should be satisfied simultaneously.

Once the bottom horizontal space vector (S_a, S_b, S_c) is calculated, all the redundant space vectors can be generated as

$$(S_{a1}, S_{b1}, S_{c1}) = (S_a, S_b, S_c) + m(1,1,1) \quad (4)$$

where integer $m \in [0, n-1-\max(S_a,S_b,S_c)]$, max($S_a$, S_b, S_c) is the maximum value among S_a, S_b and S_c.

Based on (1), (S_a, S_b, S_c) can be mapped into Fig.2(b) to obtain (S_m, S_n, S_p). Given that $\boldsymbol{OP}_1=[S_m, S_n, S_p]^T$, the origin of V_{ref2} is shifted to the detected vertex $\boldsymbol{P}_1$, which yields a "remainder vector " V_{ref3} as

$$\boldsymbol{V}_{ref3} = \boldsymbol{V}_{ref2} - \boldsymbol{OP}_1 = [V_{m1}\ \ V_{n1}\ \ V_{p1}]^T \quad (5)$$

where V_{m1}, V_{n1}, V_{p1} are normalized instantaneous remainder voltages which are simplified in coordinates m_1, $n_1$and p_1.Thus $V_{m1}=V_m-S_m$, $V_{n1}=V_n-S_n$ and $V_{p1}=V_p-S_p$.

Since the decimal vector V_{ref3} is obtained, the modulation process can be dealt with as simple as conventional two-level modulation method, as shown in Fig.3(a) and Fig.3(b).

C. Calculating D_a, D_b and D_c and obtaining the redundant switching sequences in the 3-D coordinate system

To obtain the optimized switching sequence, for the general

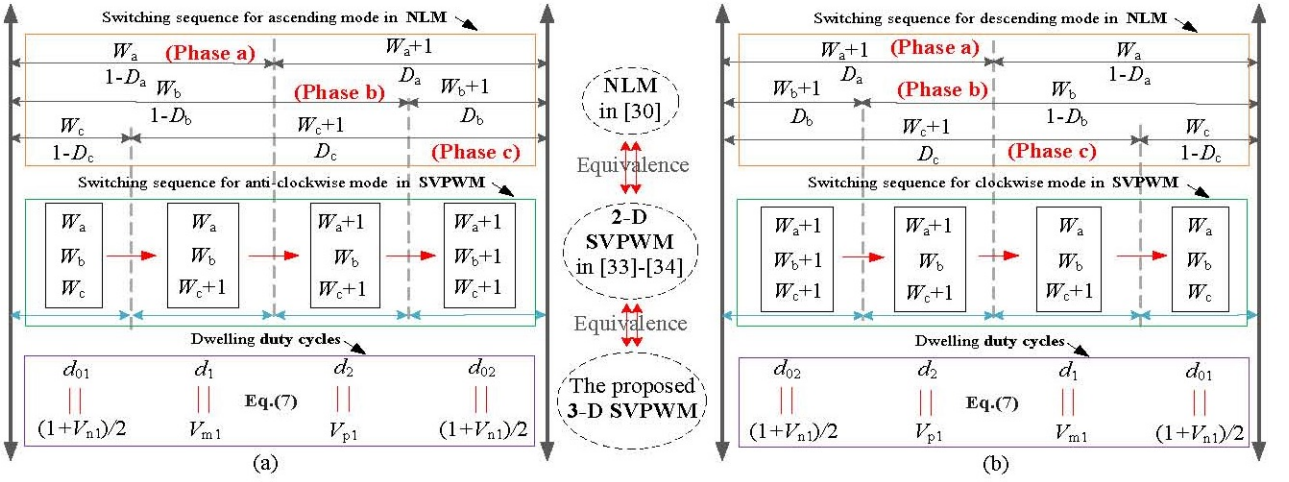

Fig.4. Switching sequences in NLM, 2-D SVPWM and 3-D SVPWM in region 5 when $d_{01}=0.5d_0$: (a) Ascending mode; (b)Descending mode.

TABLE I
COMBINATIONS OF SIGNS FOR REMAINDER VECTORS IN SIX REGIONS AND THE EQUIVALENCE OF DUTY CYCLES BETWEEN 2-D SVPWM AND 3-D SVPWM

reg	①	②	③	④	⑤	⑥
Signs	V_{m1}(+) V_{n1}(+)	V_{m1}(-) V_{p1}(-)	V_{n1}(+) V_{p1}(+)	V_{m1}(-) V_{n1}(-)	V_{m1}(+) V_{p1}(+)	V_{n1}(-) V_{p1}(-)
d_1	V_{m1}	$-V_{p1}$	V_{m1}	$-V_{m1}$	V_{m1}	$-V_{n1}$
d_2	V_{n1}	$-V_{m1}$	V_{p1}	$-V_{n1}$	V_{p1}	$-V_{p1}$
d_0	$(1+V_{p1})$	$(1-V_{n1})$	$(1+V_{m1})$	$(1-V_{p1})$	$(1+V_{n1})$	$(1-V_{m1})$

TABLE II
MAPPING OF DETERMINING SWITCHING SEQUENCE OF THE PROPOSED SVPWM METHOD WHEN $d_{01}=0.5d_0$

Sign	D_a	D_b	D_c
V_{m1}(+)&V_{n1}(+) V_{m1}(-)&V_{n1}(-)	$(1-V_{p1})/2$	$(1-V_{m1}+V_{n1})/2$	$(1+V_{p1})/2$
V_{m1}(+)&V_{p1}(+) V_{m1}(-)&V_{p1}(-)	$(1+V_{m1}-V_{p1})/2$	$(1-V_{m1}-V_{p1})/2$	$(1-V_{n1})/2$
V_{n1}(+)&V_{p1}(+) V_{n1}(-)&V_{p1}(-)	$(1-V_{n1}-V_{p1})/2$	$(1+V_{n1}+V_{p1})/2$	$(1-V_{n1}+V_{p1})/2$

TABLE III
MAPPING OF DETERMINING SWITCHING SEQUENCE OF THE PROPOSED SVPWM METHOD WHEN $d_{01}=0$

signs	D_a	D_b	D_c
V_{m1}(+)&V_{n1}(+)	1	$1-V_{m1}$	$1+V_{p1}$
V_{m1}(-)&V_{n1}(-)	0	$-V_{m1}$	V_{p1}
V_{m1}(+)&V_{p1}(+)	$1-V_{p1}$	$1+V_{n1}$	1
V_{m1}(-)&V_{p1}(-)	$-V_{p1}$	V_{n1}	0
V_{n1}(+)&V_{p1}(+)	$1+V_{m1}$	1	$1-V_{n1}$
V_{n1}(-)&V_{p1}(-)	V_{m1}	0	$-V_{n1}$

horizontal space vectors, there are two successive values defined as W_x and W_{x+1} (x=a, b and c for three phase, and 1-D_x, $D_x \in [0,1]$) in one switching cycle, as shown in Fig.3(c). Where, 1-D_x and D_x are their corresponding duty cycles based on the principle of the Nearest-Level Modulation (NLM) [35].

Given that duty cycles of V_1 and V_2 are d_1 and d_2, duty cycles of two zero vectors are d_{01} and d_{02} (d_1, $d_2 \in [0,1]$), $d_{01}+d_{02}=d_0 \in [0,1]$, which is called the total zero vector). So 1-D_x+D_x= $d_1+d_2+d_0=1$. Hence, when the simplified reference vector V_{ref3} is located in region 5 in Fig.3 (b), the general switching sequences should be from d_{01}*$W_aW_bW_c$ to d_1* W_a $W_b(W_c+1)$ to d_2*$(W_a+1)W_b$ (W_c+1) to d_{02}*(W_a+1) (W_b+1) (W_c+1) (that is from d_{01}* (0,0,0) to d_1* (0,0,1) to d_2* (1,0,1) to d_{02}* (1,1,1)) for the anti-clockwise mode and the reversed switching sequence for the clockwise mode, as shown in the green dotted box of Fig. 4. This moment, D_a is the duty cycle of W_a+1, 1-D_a is the duty cycle of W_a. Hence, the equivalence between 2-D SVPWM and NLM is generated [35]. And [32]-[34] have already concluded the interrelation between d_1, d_2, d_{01} and D_a, D_b, D_c. In this region, the anti-clockwise mode and clockwise mode in SVPWM are also called the ascending mode and descending mode in NLM.

To apply the similar equivalence to the proposed 3-D coordinate system, the next focus in this paper is to find the potential relationship between D_a, D_b, D_c and V_{m1}, V_{n1},V_{p1}. The outcome will be introduced into two subsections.

Subsection A:Identifying the regions and calculating d_1, d_2, d_{01} with V_{m1}, V_{n1},V_{p1} in the 3-D coordinate system

In order to obtain three-phase duty cycles D_a, D_b and D_c in the proposed SVPWM technique, let horizontal three vectors compassing the modulation triangle of synthesizing the reference vector be (S_{m1}, S_{n1}, S_{p1}), (S_{m2}, S_{n2}, S_{p1}) and (S_m, S_n, S_p). The corresponding duty cycles are d_1, d_2 and d_0.

Based on voltage-second equilibrium theorem [6], the following relationship can be obtained.

$$\begin{cases} V_{m1} = S_{m1}d_1 + S_{m2}d_2 + S_m d_0 \\ V_{n1} = S_{n1}d_1 + S_{n2}d_2 + S_n d_0 \\ V_{p1} = S_{p1}d_1 + S_{p2}d_2 + S_p d_0 \end{cases} \tag{6}$$

Focused back on Fig. 3(a), when V_{ref3} is located in region 5, (S_{m1}, S_{n1}, S_{p1})=(0,-1,1), (S_{m2}, S_{n2}, S_{p1})=(1,-1,0) and (S_m, S_n, S_p)=(0,0,0). Based on (6), it is acquired that

$$\begin{cases} V_{m1} = 0.d_1 + 1.d_2 + 0.d_0 = d_2 \\ V_{n1} = -1.d_1 - 1.d_2 + 0.d_0 = -(d_1 + d_2) \\ V_{p1} = 1.d_1 + 0.d_2 + 0.d_0 = d_1 \end{cases} \tag{7}$$

So $V_{m1} \geq 0$, $V_{n1} \leq 0$ and $V_{p1} \geq 0$ can be obtained in this region,

TABLE IV
SWITCHING PAIRS AND VOLTAGE BALANCING CONDITIONS IN INNER CELL

Switching pairs $\{S_1, S_2\}$	Voltage level S_x	Voltage balancing conditions
S_1=2, S_2=0	2	—
S_1=2, S_2=1	1	①: $V_{C1x}<V_{C2x}, i_{sx}>0 \| V_{C1x}>V_{C2x}, i_{sx}<0$
S_1=1, S_2=0	1	②:$V_{C1x}<V_{C2x}, i_{sx}<0 \| V_{C1x}>V_{C2x}, i_{sx}>0$
S_1=0, S_2=0	0	—
S_1=1, S_2=1	0	—
S_1=2, S_2=2	0	—
S_1=1, S_2=2	-1	③:$V_{C1x}>V_{C2x}, i_{sx}>0 \| V_{C1x}<V_{C2x}, i_{sx}<0$
S_1=0, S_2=1	-1	④:$V_{C1x}>V_{C2x}, i_{sx}<0 \| V_{C1x}<V_{C2x}, i_{sx}>0$
S_1=0, S_2=2	-2	—

they can be represented as $V_{m1}(+)$, $V_{n1}(-)$ and $V_{p1}(+)$. Reversely, $V_{m1}(-)$, $V_{n1}(+)$ and $V_{p1}(-)$ mean $V_{m1}\leq 0$, $V_{n1}\geq 0$ and $V_{p1}\leq 0$.

Similar analysis to other regions and cases, the combinations of signs of V_{m1},V_{n1} and V_{p1} in 3-D SVPWM to represent different regions and expressions of V_{m1},V_{n1} and V_{p1} to describe d_1, d_2 and d_{01} are respectively included in Table I.

Therefore, according to Table I, the switching sequences mentioned above in region 5 of 2-D SVPWM diagram in Section II-C have an alternative description, that is, from $((1+V_{n1})/2)^*$ $W_aW_bW_c$ to V_{m1}^* $W_aW_b(W_c+1)$ to V_{p1} $^*(W_a+1)W_b$ (W_c+1) to $((1+V_{n1})/2)$ $^*(W_a+1)$ (W_b+1) (W_c+1)" in the proposed 3-D SVPWM for the anti-clockwise mode and vice verse. Obviously, the equivalence between 2-D SVPWM and 3-D SVPWM has achieved, as shown in Fig.4.

Subsection B: Finding the potential relationship between V_{m1}, V_{n1},V_{p1} and D_a, D_b, D_c.

Further to get more degrees of freedom for the proposed 3-D SVPWM scheme, two tables are deduced to map the relationship between 3-D SVPWM and NLM.

Having known that D_a, D_b and D_c can be expressed by d_1, d_2, d_{01}. d_1, d_2, d_{01} can be also expressed by V_{m1}, V_{n1}, V_{p1} based on (6) and (7). Hence, V_{m1}, V_{n1} and V_{P1} can be used to directly get the duty cycles, D_a, D_b and D_c, which acquires another equivalence between 3-D SVPWM and NLM.

It is known that D_a=1-d_{01}-d_1, D_b=1-d_{01}- d_1-d_2 and D_c=1-d_{01} in region 5 [33]. Then joint Table I, the following relationship can be acquired.

$$\begin{cases} D_a = (1+V_{m1}-V_{p1})/2 \\ D_b = (1-V_{m1}-V_{p1})/2 \\ D_c = (1-V_{n1})/2 \end{cases} \tag{8}$$

According to the symmetry of the space-vector diagram, so D_a, D_b and D_c in region 2 have the identical expressions based on (8). By that analogy, the mapping of determining the switching sequences in different regions of the proposed 3-D SVPWM technique for the continuous mode is obtained in Table II.

For the discontinuous mode (d_{01}=0), because zero vector has different redundant expressions, either (0,0,0) or (1,1,1) in two relative regions, e.g. (1,1,1) in region 2 and (0,0,0) in region 5, the relationship between D_a, D_b, D_c and V_{m1}, V_{n1}, V_{p1} has different expressions in two relative regions. Similarly based on Table I to Table II, the mapping of determining the switching sequences for this mode is generated as Table III. By the way, the SVPWM wave in this mode will not be symmetrical in two half periods due to asymmetrical discontinuous areas enclosed

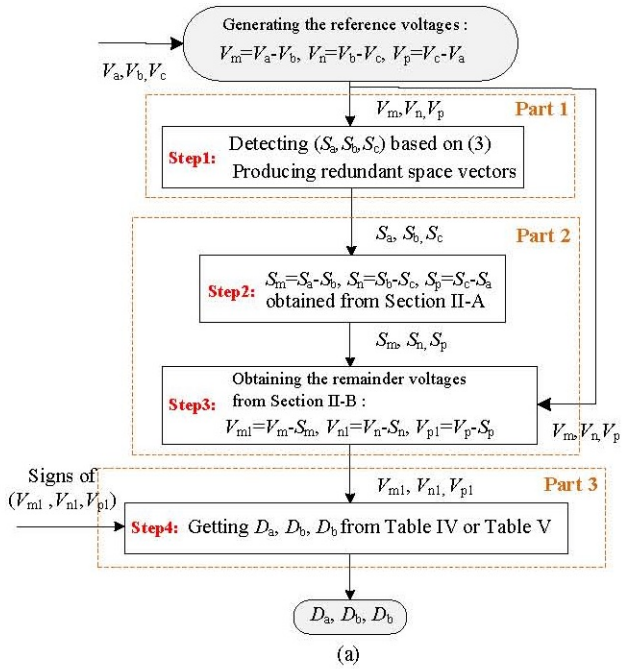

Fig.5. Flowchart of the proposed SVPWM method.(a) Flowchart of the 3-D NLM-Based SVPWM Technique, (b) Flowchart of the voltage balancing algorithm using the NLM-Based principle.

by the duty cycles in two adjacent half switching periods.

This another equivalence confirms the interrelationship between 3-D SVPWM algorithm and NLM algorithm.

D.Summarizing the whole implemented process of the Proposed 3-D SVPWM scheme

As aforementioned, the process of the proposed SVPWM algorithm is summarized in Fig.5.

Visibly, the SVPWM can be generated by three parts including four steps.

To better describe this flowchart, an example is given. When

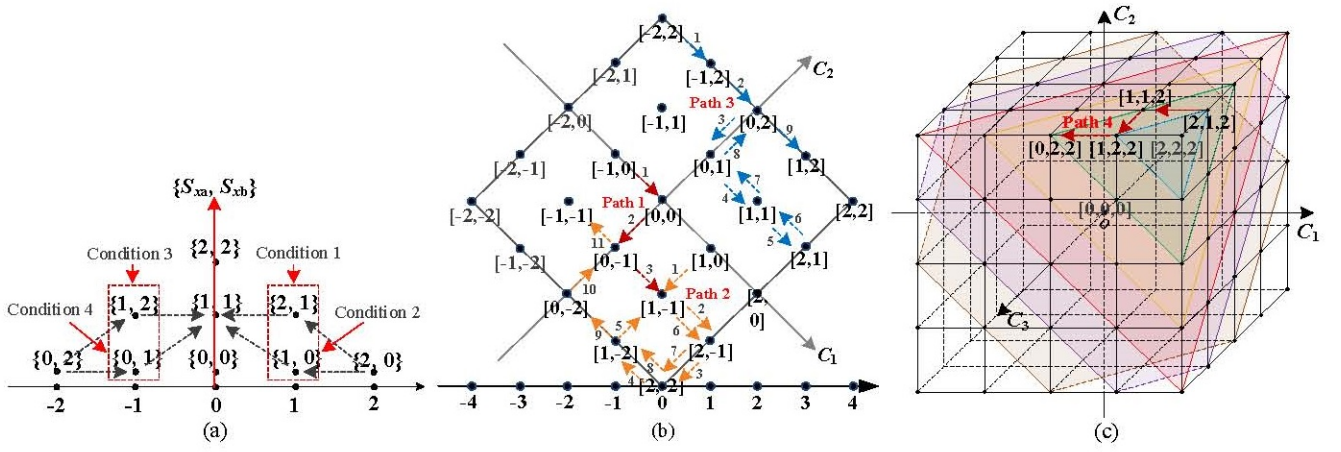

Fig.6. Switching pairs and vertical space vector transition in *n*-D plane to balance inner-cell and mutual cell.(a) Switching pairs transition in 1-D plane, (b) Vertical space vector transition for two cascaded cells in 2-D plane, (c) Vertical space vector transition for three cascaded cells in 3-D plane.

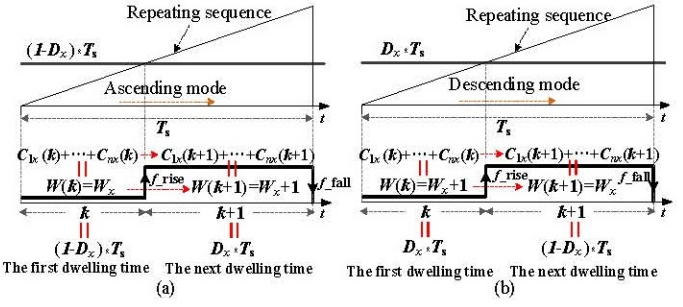

Fig.7. Allocation of time for different voltage levels in one duty cycle. (a) Ascending mode.(b) Descending mode.

reference vector is located in the Area 3, as shown in Fig.2(a), the amplitudes of V_m, V_n and V_p approximately take values of 2.2, -3.6 and 1.6. Based on (3), the bottom horizontal space vector (S_a, S_b, S_c) = (2,0,3) is detected. Then (S_m, S_n, S_p)=(S_a-S_b, S_b-S_c, S_c-S_a)=(2, -3,1). Furthermore V_{m1}, V_{n1} and V_{p1} can be obtained from V_m-S_m=0.2, V_n-S_n=-0.6 and V_p-S_p=0.6. Finally, when continuous mode is operated, three duty cycles D_a=(1+V_{m1}-V_{p1}) /2=0.3, D_b=(1-V_{m1}-V_{p1})/2=0.1, D_c= (1-V_{n1})/2= 0.8 can be obtained.

From the modulation process, it is obvious that the simple sign judgments and arithmetic calculations in the proposed algorithm can help to realize the reduced computational complexity.

III. Equalizing the Unbalanced Voltages Using The NLM-Based Principle for 3LNPC Cascaded Converter

For the 3LNPC cascaded multilevel converter shown in Fig.1, unbalanced voltages V_{C1x}, V_{C2x} in inner cell and V_{dcx1}, V_{dcx2}, …, V_{dcxn} in mutual cell in each phase are the inherent issue need to be addressed. Based on the proposed 3-D NLM-based SVPWM, the unbalanced voltages can be equalized.

A. Equalizing the unbalanced voltages in inner cell

As shown in Fig.1, considering about the switching pairs {S_{1x}, S_{2x}}, as shown in Fig.1(b). There are altogether 9 switching pairs in inner cell. Because one cell consists of two 3-level (3L) arms. According to the operation principle of the 3L diode -clamped circuit [7], one arm switching function S_z is defined as

$$S_z=\begin{cases}2, & S_{x11}\ \text{on},\ S_{x21}\ \text{on}\\ 1, & S_{x21}\ \text{on}, S_{x31}\ \text{off}\\ 0, & S_{x11}\ \text{off}, S_{x21}\ \text{off}\end{cases} \tag{9}$$

where, z=1,2; x=a, b, c.

Similar definition is suitable for another arm.

In (9), S_z can be taken 0~2 according to different switching devices state combinations. Thus, voltage level W_x=S_1-S_2. Hence The values 0~4 of W_x can be reconstructed as -2~2 for a cascaded multilevel converter, as shown in Table IV. It can be seen that when voltage level W_x =1 or -1, there are several redundant switching pairs. Among those, which one should be applied depends on different voltage balancing conditions. For example, when W_x =1, switching pairs {2, 1} is applied under the condition: V_{C1x}<V_{C2x}, i_{sx}>0||V_{C1x}>V_{C2x}, i_{sx}<0. This moment, C_{1x} is charged when i_{sx} >0 or C_{1x} is discharged when i_{sx}<0 to achieve the dynamically balance between V_{C1x} and V_{C2x} based on the corresponding switching states of switching devices from (9). Similarly, when W_x= -1, switching pairs {1, 2} is applied under the condition: V_{C1x}>V_{C2x}, i_{sx}>0 || V_{C1x}<V_{C2x}, i_{sx}<0. It can be also understand that when V_{C1x}>V_{C2x}, i_{sx}>0, switch pairs {1, 2} will drive switching devices S_{x21}, S_{x31} and S_{x51}, S_{x61} in on-state to discharge capacitor C_{1x} and lower the voltage V_{C1x} for the balance with V_{C2x}. This idea is generally suitable for other conditions.

Switching pairs transition in 1-D plane is finally included in Fig.6(a). In order to minimize the number of switching transition, when W_x=0, switching pairs {1,1} should be applied.

B. Equalizing the unbalanced voltages in mutual cell

Define the general form of vertical space vector as [C_{1x}, C_{2x},..., C_{hx}] for phase x to form h-D plane and general voltage level as W, as shown in Fig. 6(b) and Fig. 6(c), where h is the number of power cells and takes h ≥2; C_{1x}, C_{2x} ,..., C_{nx} are respectively the output levels for cell 1 to Cell n in x phase. They can be obtained by port voltages V_{x1}/V_{dc}, V_{x2}/V_{dc} ,..., V_{xn}/V_{dc}. Hence, it is clear that the general voltage level W=W_x or W=W_x+1 is equal to C_{1x}+C_{2x}+...+C_{hx} in different dwelling times. Taking the cascaded converter with two cells as an example, when W_x or W_x+1= -2, there are three redundant vertical space

vectors, [-2,0], [-1,-1] and [0,-2], for -2+0= -1+(-1)=0+(-2)= -2, as shown in Fig.6(b).

Fig.7 shows the allocation of time in one duty cycle. In Fig.7, the addition of interval k and interval k+1 is a duty cycle, i.e., k+(k+1)=T_s. They are also respectively taken as the first dwelling time and the next dwelling time during one duty cycle T_s. They are equal to (1-D_x)*T_s and D_x*T_s since the equivalence between the proposed 3-D SVPWM and the NLM has been achieved

Define the timing sequence and the related variables W, V_{dc1} to V_{den}, C_{1x} to C_{nx} at k interval as $W(k)$, $V_{dc1}(k)$ to $V_{dc2}(k)$, $C_{1x}(k)$ to $C_{nx}(k)$ and at k+1 interval as $W(k+1)$, $V_{dc1}(k+1)$ to $V_{dc2}(k+1)$, $C_{1x}(k+1)$ to $C_{nx}(k+1)$. In a duty cycle, voltage level W may be changed from W_x to W_x+1 or from W_x+1 to W_x, as mentioned above. Hence, for the vertical space vector [C_{1x}, C_{2x},..., C_{hx}], only one of them changes with one unit value in a duty cycle. The variation moments are respectively marked as "*f*=*f*_rise" and "*f*=*f*_fall".

For example, when ascending mode is operated, if C_{1x} changes with one unit value at k+1 interval, that is $C_{1x}(k+1)=C_{1x}(k)+1$, then C_2 to C_{nx} will remain unchanged, that is, $C_{2x}(k+1)=C_{2x}(k)$ ... $C_{nx}(k+1)=C_{nx}(k)$, which corresponds to the variation of W from W_x to W_x+1. Similarly, when descending mode is operated, $C_{1x}(k+1)=C_{1x}(k)-1$ and $C_{2x}(k+1)=C_{2x}(k)$, ... $C_{nx}(k+1) = C_{nx}(k)$, which corresponds to the variation of W from W_x +1 to W_x. This idea can be applied to address the unbalanced voltages in 3LNPC-CMC with minimum number of switching transition. That will be introduced next.

For a two cascaded cell converter, generally assuming the average value of V_{dcx1} and V_{dcx2} as V_{ave2x} (V_{ave2x} =(V_{dcx1}+V_{dcx2})/2).

If there exists the dc unbalanced voltage condition V_{dcx1} (k) >V_{ave2x}, V_{dcx2}(k) < V_{ave2x} and i_{sx} (k)>0, based on the law of conservation of energy, C_{1x}(k) should be reduced or C_{2x}(k) should be raised at k+1 interval to achieve the balance between V_{dcx1}(k+1) and V_{dcx2}(k+1) at k+1 interval, i.e., V_{dcx1} (k+1) is approximately equal to V_{dcx2} (k+1).

Hence, when voltage level W(k) changes from W_x+1 at k interval to W_x at k+1 interval, C_{1x} can be firstly reduced with unit value, i.e. C_{1x} (k+1)= C_{1x} (k)-1 and C_{2x} remains unchanged at k+1, that is C_{2x} (k+1)= C_{2x} (k). Inversely, when ascending mode is operated, C_{2x} (k+1) = C_{2x} (k)+1 and C_{1x} (k+1) = C_{1x} (k).

Therefore, the unbalanced voltages V_{dcx1} and V_{dcx2} can be achieved equalized in real time due to the corresponding variation of C_{1x} and C_{2x}. Because only one of C_{1x}, C_{2x} is changed between two dwelling times during voltage balancing process, the minimum number of switching transition is guaranteed.

Summarily, define C_{1xstep} as the variation value of C_{1x} from k interval to k+1 interval, under different voltages unbalanced conditions, when ascending more is operated, C_{1xstep} takes

$$C_{1xstep}=\begin{cases}+1 & V_{dcx1}<V_{ave2x},\ i_{sx}>0 \,||\, V_{dcx1}>V_{ave2x},\ i_{sx}<0\\ 0 & V_{dcx1}>V_{ave2x},\ i_{sx}>0 \,||\, V_{dcx1}<V_{ave2x},\ i_{sx}<0\end{cases} \quad (10)$$

When descending mode is operated, C_{1xstep} takes

$$C_{1xstep}=\begin{cases}0 & V_{dcx1}<V_{ave2x},\ i_{sx}>0 \,||\, V_{dcx1}>V_{ave2x},\ i_{sx}<0\\ -1 & V_{dcx1}>V_{ave2x},\ i_{sx}>0 \,||\, V_{dcx1}<V_{ave2x},\ i_{sx}<0\end{cases} \quad (11)$$

Based on above analysis, an example is given, if [C_{1x} (k), C_{2x} (k)]= [-1,0] and W(k) will changes with +1 at k+1 interval, i.e., W(k+1)=-1+1=0. When there exists V_{dcx1}(k) <V_{dcx2}(k) i_{sx} (k)>0, C_{1xstep} will be equal to +1 based on (10) and C_{1x}(k+1) = C_{1x} (k) + C_{1xstep}= -1+1=0. C_{2x}(k+1) is equal to W(k+1) -C_{1x}(k+1)=0-0=0. Finally, [C_{1x}(k+1), C_{2x}(k+1)] = [0,0]. Continuing the calculation and based on Fig.3(c), the vertical space vector transition sequence will be from D_x*[0,0] to (1-D_x)*[0,-1] to D_x*[1,-1], marked as path 1 in Fig.6(b).

Finally, Table IV is applied along with the sequence to address the unbalanced voltages in inner cell dynamically.

Using the same principle to three cascaded cells system, if there exists V_{dcx1}>V_{avex}, V_{dcx2}>V_{avex}, V_{dcx3}>V_{avex} and i_{sx} >0, when [C_{1x}(k), C_{2x}(k), C_{3x}(k)]=[2,1,2], based on similar analysis with (10) and (11), [C_{1x}(k+1), C_{2x}(k+1), C_{3x}(k+1)] will be equal to [1,1,2] at k+1 interval. Ultimately, the vertical space vector transition sequence can be from D_x*[2,1,2] to (1-D_x)*[1,1,2] to D_x*[1,2,2] to (1-D_x)*[0,2,2], marked as path 4 in Fig.6(c).

As discussed above, based on the NLM-based principle, the variation of voltage level in each phase can reflect the variation of port level for each cell, which finally can be applied to address the mutual-cell unbalanced voltages in the cascaded multilevel converter. In addition, owing that the variation of voltage level may be less than |1| and the variation point is fixed at "*f*=*f*_rise" or "*f*=_fall", the minimum number of switching transition and the fixed switching frequency can be guaranteed simultaneously.

The whole process of voltages balancing for more cascaded cells system is also shown in Fig.5(b).

IV. Simulation and Experimental Results

A. Simulation Results

To verify the proposed algorithm, a n-level multilevel converter was simulated in Matlab/Simulink to demonstrate the performance of the proposed SVPWM scheme. The parameters are: dc source is 100V, the switching frequency is 5kHZ. Inductive Load: R=20Ω, L=10mH; C_{1x}=C_{2x}=470uF.

Fig.8 (a) shows online variation of phase voltage and line voltage waveforms under varied modulation index from 0.5 to 0.85 and switching frequency from 2kHz to 5kHz when five-level converter is applied, i.e. one power cell is applied.

Fig.8 (b) describes the online variation of d_{01} from 0.5*d_0 to 0 when d_{01}=0.5*d_0. To present all the redundant horizontal space vectors, with relatively low modulation index, the detected horizontal space vector will be selected as the second horizontal space vector for the ascending mode in one switching cycle and the bottom horizontal space vector for the reverse mode in next switching cycle. For example, if the reference voltage is in triangle T_1 (Fig.2(a)), The detected vertex is Q_{21}, the switching sequence is from (3,3,1) to (3,4,1) to (4,4,1) to (4,4,2) for the ascending mode when m=1 in one switching cycle and from (3,3,1) to (3,3,0) to (2,3,0) to (2,2,0) for the descending mode when m=0. Obviously, the normalized level of the phase is from 3 to 4 to 3 to 2, alternately changed every other switching cycle, which are marked in Fig.8 (b). Whereas, when d_{01}=0, the discontinuous modulation output appears and the line voltage still keep presenting 7-level output. The discontinuous result is not symmetrical in two half periods due to the asymmetrical discontinuous areas enclosed by

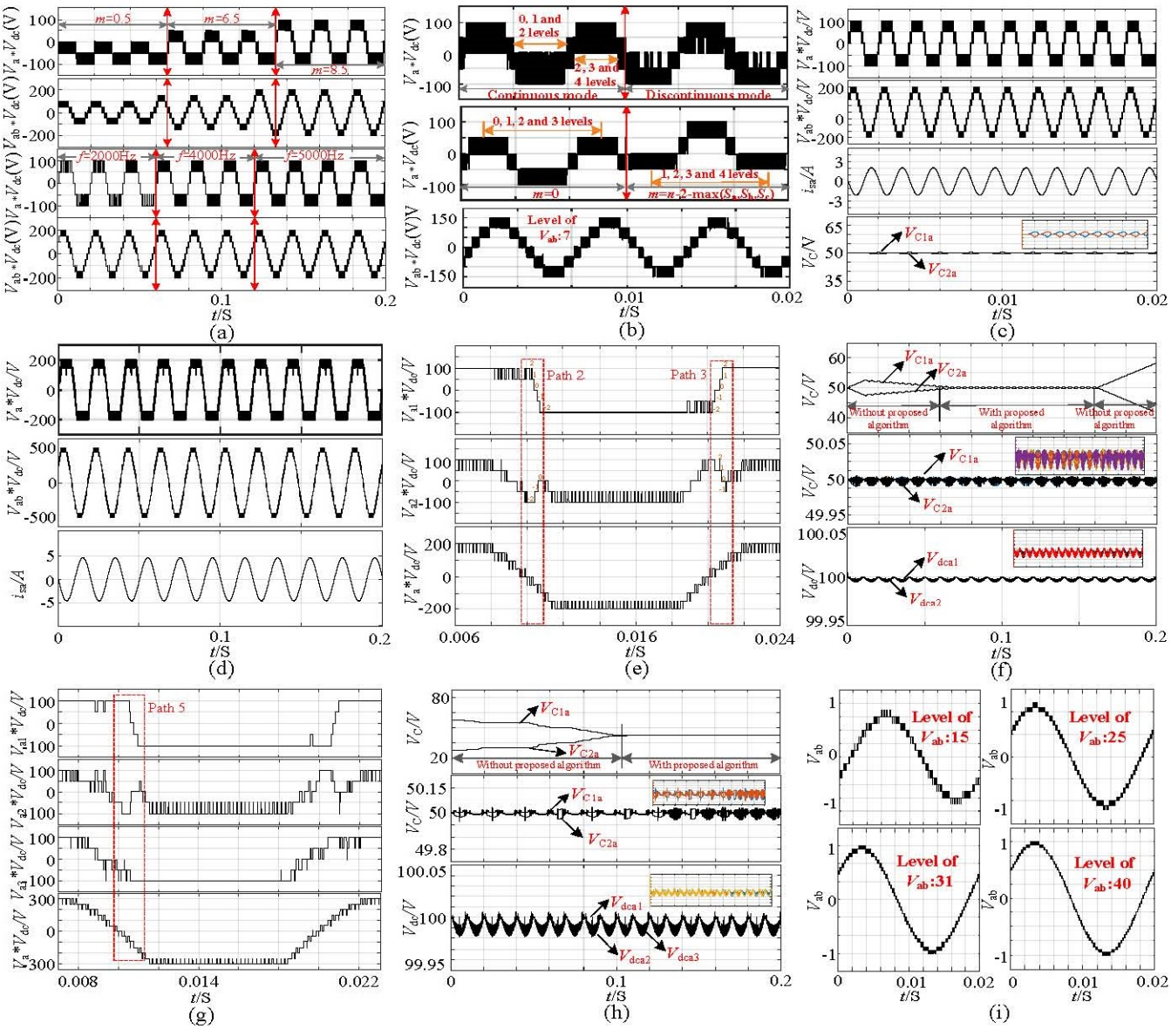

Fig.8. Simulation Results.(a) waveforms of phase voltage and line voltages at different modulation indexes and switching frequencies, (b)Different operation modes and their SVPWM generations, (c) Five-level voltages output with the balanced voltages in inner cell, (d) Nine-level voltages output, (e)-(h) Voltages balancing in inner cell and mutual cell with minimum number of switching transition in each cell for a two cascaded system and a three cascaded system, (i) More voltage levels output for line voltages.

discontinuous duty cycle in adjacent two periods. It can be seen that redundant space vectors can be selected flexibly to generate the redundant switching sequences. Meanwhile, different modulation modes can be achieved easily.

The waveform to illustrate the unbalanced voltages in inner cell is shown in Fig.8 (c). The unbalanced voltages V_{C1a} and V_{C2a} can be equalized by the proposed algorithm described in Section III-A and Table IV.

As shown in Fig.8 (d) to Fig.8 (f). The issue of unbalanced voltages in inner cell and mutual cell can be addressed simultaneously with the minimum number of switching transition in two cascaded power cell system based on the method in Section III-B. The transition path is from [1,0] to [1,-1] to [2,-1] to [2,-2] to [1,-2] to [1,-1] to [2,-1] to [2,-2] to [1,-2] to [0,-2] to [0,-1] to [-1,-1], marked as Path. 2. Similar analysis can be applied for Path 3. Obviously, Based on the NLM-based SVPWM algorithm and voltage balancing principle, the output level $[C_1, C_2]$ is ensured transitive with a unit value of one of two power in one duty cycle, which can reduce the switching devices loss. This moment, the phase voltage is normally 9-level and the line voltage is 17-level. Because of the inductive load, the phase current i_{sa} presents sinusoidal output.

Fig.8(g) and Fig.8(h) illustrate 13-level output for three cascaded power cells. The level transition path is from [2,-2,-1] to [2,-2,-2] to [2,-2,-1] to [1,-2,-1] to [1,-2,0] to [1,-1,0] to [0,-1,0], marked as Path 5. Meanwhile, the voltages in inner cell and mutual cell can be balanced. When the proposed algorithm is dislodged, the voltages will spread out.

A 15-level, 25-level, 31-level and 40-level outputs is shown in Fig.8 (i) to verify the flexibility and extensibility of the proposed method.

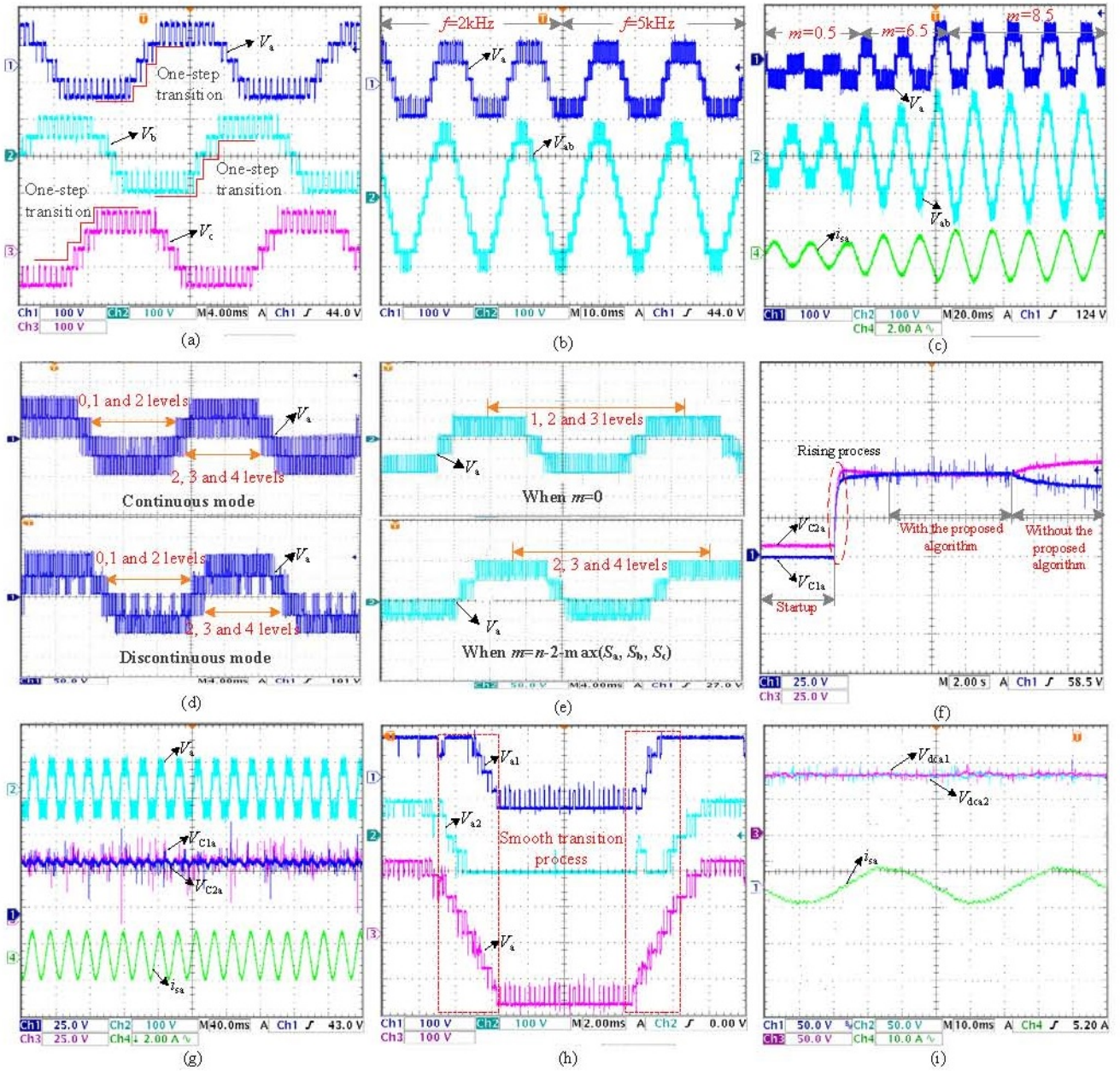

Fig.9. Experimental results.(a) Three-phase voltages, (b) Phase voltage and line voltage with different switching frequencies, (c) Phase voltage, line voltage and phase current, (d) and (e) SVPWM output in different modes, (f) Voltages in inner cell in dynamic state, (g) balanced inner-cell voltages and the phase voltage and phase current in steady state, (h) Nine-level voltage output, (i) Unbalanced voltages in mutual cell.

B. Experimental Results

A small-scale experimental setup is implemented using the same parameters of simulation. A master-slave control mode is applied. The proposed algorithm is totally coded using Verilog-HDL, synthesized using Quartus II and programmed onto the master FPGA controller: EP3C55F484C7 and the slave FPGA controller: EP1C12Q240C8. The machine of single DC power supply is ITECH IT6726V.

Fig.9 (a) shows the waveform of three-phase voltages V_a, V_b and V_c. It can be seen that the phase voltages are achieved one-step transition to guarantee the low voltage stress during the modulation process.

The online variation of switching frequency and modulation index for a five-level cascaded converter are presented in Fig.9 (b) and Fig.9 (c), which corresponds to the simulation results in Fig.8(a). Visibly, the phase voltage and the line voltage have good dynamic present at different switching frequencies. When the modulation index is varied in real time, the level number of phase voltage and line voltage can be flexibly changed along with it. Hence, the proposed algorithm is suitable for any level of multilevel converters at different working frequencies.

Fig.9 (d) illustrates the experimental results of different modulation modes under different m values. Based on the identical example listed in "Simulation section", with relatively low modulation index, the PWM outputs are four levels. On the premise of S_a=2, when m=1 is taken for the ascending mode and m=0 is taken for the descending mode, the normalized level of the phase is from 3 to 4 to 3 to 2. Furthermore, at a power

TABLE V
THE COMPARISON BETWEEN THE PROPOSED SVPWM METHOD AND THE EARLIER SVPWM METHODS IN FIVE-LEVEL TOPOLOGY IN DIFFERENT ASPECTS

SVPWM Techniques	Optimized Switching Sequences	Adjustable Duty Cycles	Region & Triangle Identification	*m* Factor	Dividers	Multipliers	Trigonometric Functions	Time Required (ns)	Memory Bytes
In [17]	Generated	—	Calculation	—	6	0	0	4200	22548
In [23]	Generated	—	Signs	—	0	0	0	553	0
In [24]	Generated	—	Calculation	Provided	4	1	2	618	2468
In [25]	Look-up table	—	Calculation	—	3	5	2	3450	49802
In [27]	Look-up table	—	Judgment	—	0	0	0	244	8172
In [31]	Look-up table	—	Signs	—	1	3	0	726	4224
In [35]	Generated	—	Matrix	—	0	2	0	1890	8172
In [32]	Look-up table	Provided	Calculation	—	5	8	2	992	9732
In [33]	Generated	Provided	Calculation	Provided	4	6	2	594	5768
In [36]	—	—	Sign	Provided	0	0	0	433	0
The proposed	Generated	Provided	Sign	Provided	0	0	0	226	0

"—" represents "Not provided".

TABLE VI
FURTHER COMPARISON IN RESOURCES UTILIZATION

SVPWM Techniques	Logical Cell	Dedicated Logic Registers	Real-time computation
In[23]	2370	2269	Guaranteed
In[33]	1379	1225	Not guaranteed
In the paper	481	243	Guaranteed

frequency duty cycle, the normalized level will be from 1 to 0 to 1 to 2 to 3 to 4 to 3 to 2. This results are consistent with the simulation results in Fig.8 (b). It is verified again that the redundant property and different modulation modes can be easily obtained by the proposed algorithm.

m factor applied to achieve different PWM outputs can be also illustrated in Fig.9(e).

Fig.9 (f) shows the dynamic transition process of V_{C1a} and V_{C2a}. At startup, capacitors C_{1a} and C_{2a} have different initial voltages. With the proposed algorithm, it is obvious that V_{C1a} and V_{C2a} are balanced. Then when the proposed algorithm is disposed of, voltages of C_{1a} and C_{2a} dispread rapidly. So the voltage balancing capability of the introduced voltages balancing algorithm is demonstrated.

Voltages balancing effectiveness in steady state with the proposed algorithm is indicated in Fig.9(g). This moment, the sinusoidal current and regular phase voltage can be obtained.

Fig.9 (h) and Fig.9 (i) show experimental waveforms of voltage balancing effectiveness in inner cell and in mutual cell simultaneously. It is seen that V_{dca1}, V_{dca2} are balanced and voltages V_{a1}, V_{a2} are irregular to present one-stage transition, which corresponds to the simulation results. Obviously, the issue of unbalanced voltages is addressed and thus the minimum number of switching transition can be achieved.

C. Comparison with the existing well-know SVPWM methods

Subsection A:Comparison in the digital implementation

Table V lists the detailed digital implementation comparison among different SVPWM techniques.

In the aspect of digital calculation implementation, many SVPWM techniques in [24]-[25], [32]-[34] rely on some complex arithmetic calculations in which dividers, multipliers and trigonometric functions are applied. Yet the proposed one involves none of these calculations.

In view of the required time for the digital implementation and the memory resources, 2.26*e-7 seconds and the zero bytes are respectively required for the proposed SVPWM technique, which is obviously the fastest and the most hardware efficient among the existing SVPWM methods. To identify the region and triangle of the space-vector diagram, techniques in [17], [24], [25], [32] and [33] require a 2-level or *n*-level multiplication and division calculations. Technique in [27] requires corresponding comparison. The proposed one omits these kinds of calculations. Only the signs judgment of related variables are required.

In terms of improving the potential performance of multilevel converters, the proposed algorithm and the algorithm in [33] both provide the *m* factor which can be applied for more actual applications. Meanwhile, the optimized switching sequences and adjustable duty cycles are automatically guaranteed with the theories of the proposed algorithm. Whereas, the techniques in [23], [25], [31] and [32] should apply extra look-up tables to get the corresponding effectiveness. Thus the technique in [36] do not directly determine the optimized switching sequence. In addition, techniques in [17]-[31] and [35] and [36] cannot flexibly determine the duty cycles to acquire different operational modes (continuous and discontinuous modes).

Table VI lists further comparison in resources utilization to verify the digital utilization benefits of the proposed SVPWM scheme. In terms of the real-time computation, the digital implementation of the proposed SVPWM method can be easily executed online. Meanwhile its computational accuracy can be guaranteed. Nevertheless, the method in [33] needs the memory modules. Therefore there is a compromise in the memory resources and the accuracy for the method in [33]. If the accuracy is prior preferential, there will be a certain amount of memory bytes required，as shown in Table V. Inversely, if the offline calculation is executed, the computational accuracy will be reduced.

Subsection B:Comparison in the actual application

Table VII lists the detailed actual application comparison among different SVPWM techniques.

In view of the voltage balancing capability, algorithms in [17], [31] and[35] do not consider the voltage balancing capability. Whereas, [23], [33], [36] and this paper discuss the.

TABLE VII
THE COMPARISON BETWEEN THE PROPOSED SVPWM METHOD AND THE EARLIER SVPWM METHODS IN ACTUAL APPLICATIONS

SVPWM Techniques	Voltage balancing capability	Common-voltage reduction	Harmonic Performance Optimizing	Switching loss
In [17]	Not considered	Not considered	THD of current:2.3% and of voltage <25% in three-level NPC	Not considered
In [23]	By optimizing switching sequence in NPC	Not considered	Not considered	Not considered
In [31]	Not considered	By optimizing switching sequence and duty cycles in CHB	THD of current:4.38% and THD of voltage :22% in five-level CHB	Not considered
In [35]	Not considered	Not considered	THD of current:2.5% and THD of voltage :19.9% in five-level NPC	Not considered
In [32]	Not included in actual applications	Not considered	THD of current:2.32% and THD of voltage :20.4% in five-level CHB	Not considered
In [33]	By optimizing switching sequence in MMC	Discussed	Discussed	Considered
In [36]	By optimizing switching sequence in ANPC	By optimizing switching sequence in ANPC	Not considered	Not considered
The proposed	By optimizing level transition in CHB	Discussed	THD of current:1.23% and THD of voltage :17.3% in five-level CHB	Considered

"NPC", "ANPC" and "CHB" represent "Neutral-point Clamped Converter", represents " Active Neutral-point Clamped Converter" and "Cascaded H-bridge.

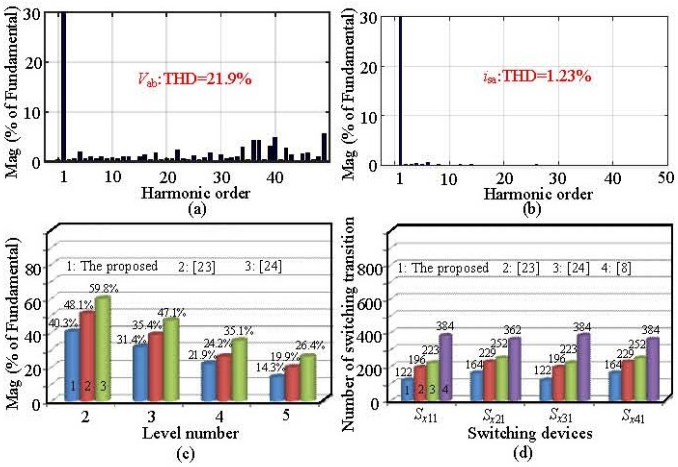

Fig.10. Comparison in Harmonic performance and switching loss. (a) and (b) THD of line voltage and phase current in four-level output. (c) Comparison in harmonic performance for different SVPWM methods, (d) Number of switching transition for different SVPWM methods.

voltage balancing capability of the SVPWM methods in different multilevel topologies.

For the aspect of the common-voltage reduction, [31] and [36] have introduced control strategies to reduce the common voltage. For the capability of optimizing harmonic performance, compared with other SVPWM techniques, the techniques in [17], [33], [35] and the proposed algorithm can flexibly achieve the choice of different switching sequences, which may easily obtains the harmonic benefits. Thus, with the proposed algorithm, the THD of the line voltage and the load current are respectively 17.3% and 1.23% shown in Fig.10(a) and Fig.10(b), which are comparable with that obtained using other existing SVPWM methods, visible in Fig.10(c).

In terms of the switching loss, as shown in Fig.10(d), owing that optimized and redundant switching sequences are provided by the proposed algorithm, even when addressing the unbalanced voltages in 3LNPC-CMC, the number of switching transition can reach minimum which lower the switching loss to an extreme. However, the method s in [23], [24] and [8] have a distinct increase in number of switching transition compared with the proposed one. Especially for the carrier-shift modulation technique in [8], more numbers of carrier wave are needed with the level number increasing to compared with the modulation wave.

Obviously, the comprehensive comparison in different aspects with existing SVPWM methods confirms the superiority of the proposed technique.

V. CONCLUSION

A three-phase simplified 3-D NLM-based SVPWM method is proposed in this paper. Compared with the generalized 2-D NLM-based SVPWM algorithms, the real-time PWM wave is generated by the proposed algorithm in reduced steps. Hence, the salient advantage of the 3-D NLM-based SVPWM method is reflected in the digital implementation. Its whole modulation process is independent of level numbers and fully eliminates complex arithmetic calculations. Virtually, several real-time addition and subtraction calculations are required and executed, which presents the better digital implementation and lower hardware occupancy.

In addition, according to the NLM-based characteristic, an optimized voltage balancing modulation algorithm is introduced to address the unbalanced voltages in inner cell and mutual cell with the minimum number of switching transition for a 3LNPC-CMC.

Finally, the further comprehensive comparison in different aspects with the existing SVPWM methods confirms its superiority.

References

[1] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[2] S. Kouro et al., "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, [1] Aug. 2010.

[3] M.Saeedifard, R.Iravani, and J.Pou,"Analysis and control of DC capacitor-voltage-drift phenomenon of a passive front-end five-level converter,"*IEEE Trans. Ind. Electron.*, vol.54, no. 6,pp.3255-3266, Dec. 2007.

[4] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25,no. 4, pp. 2903–2912, Oct. 2010.

[5] I.Ahmed, V.B. Borghate, A.Matsa, P.M.Meshram, H.M.Suryawanshi and M.A.Chaudhari,"Simplified space vector modulation techniques for multilevel inverters," . *IEEE Trans. Power Electron.*,vol.31,no.12, pp,8483-8499,Dec. 2016.

[6] Y. Deng, M. Saeedifard, and R. G. Harley, "An optimized control strategy for the modular multilevel converter based on space vector modulation," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*,Mar. 2015, pp. 1564–1569.

[7] H.J.Lin, Z.L.Shu, X.Q.He and M.Liu, N-D SVPWM With DC Voltage Balancing and Vector Smooth Transition Algoirthm for a Cascaded Multilevel Converter[J]. *IEEE Trans. Ind. Electron*., vol.65, no.5,pp. 3837-3847, May,2018.

[8] S. Sahoo and T. Bhattacharya, "Phase shifted carrier based synchronized sinusoidal PWM techniques for cascaded H-bridge multilevel inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 513–524, Jan. 2018.

[9] W. Yao, H. Hu, and Z. Lu, "Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter," IEEE Trans. Power *Electron.*, vol. 23, no. 1, pp. 45–51, Jan. 2008.

[10] A. Gupta and A. Khambadkone, "A simple space vector PWM scheme to operate a three-level NPC inverter at high modulation index including overmodulation region, with neutral point balancing," *IEEE Trans. Ind.Appl.*, vol. 43, no. 3, pp. 751–760, May/Jun. 2007.

[11] O. Dordevic, E. Levi, and M. Jones, "A vector space decomposition based space vector PWMalgorithm for a three-level seven-phase voltage sourceinverter," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 637–649, Feb.2013.

[12] .R.Maheshwari, S. Busquets-Mong, and J. Nicolas-Apruzzese,"A novel approach to generate effective carrier-based pulse width modulation strategies for diode-clamped multilevel DC-AC converter". *IEEE Trans. Power Electron*., vol.63,no.11,pp.7243-7252,Nov.2016.

[13] Y. Deng, M. Saeedifard, and R. G. Harley, "An improved nearest-level modulation method for the modular multilevel converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2015, pp. 1595–1600.

[14] J. I. Leon *et al.*, "Conventional space-vector modulation techniques versus the single-phase modulator for multilevel converters," *IEEE Trans. Ind .Electron.*, vol. 57, no. 7, pp. 2473–2482, Jul. 2010.

[15] A. Gupta and A. Khambadkone, "A simple space vector PWM scheme to operate a three-level NPC inverter at high modulation index including overmodulation region, with neutral point balancing," *IEEE Trans. Ind.Appl.*, vol. 43, no. 3, pp. 751–760, May. 2007.

[16] H. Zhang, S. Finney, A. Massoud, and B.Williams, "An SVM algorithm to balance the capacitor voltages of the three-level NPC active power filter,"*IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2694–2702, Nov. 2008.

[17] P.Chamarthi,P.Chhetri, and V. Agarwal,"Simplified implementation scheme for space vector pulse width modulation of n-level inverter with online computation of optimal switching pulse durations," *IEEE Trans. Ind. Electron*., vol.63,no.11,pp.6695-6704,Nov.2016.

[18] Y. Deng, K. H. Teo, and R. G. Harley, "Generalized DC-link voltage balancing control method for multilevel inverters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2013, pp. 1219–1225.

[19] O. Lopez, J. Alvarez, J. Doval-Gandoy, and F. D. Freijedo, "Multilevel multiphase space vector PWM algorithm," *IEEE Trans. Ind. Electron*., vol. 55, no. 5, pp. 1933–1942, May 2008.

[20] B. P. McGrath, D. G. Holmes, and T. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron.*,vol. 18, no. 6, pp. 1293–1301, Nov. 2003.

[21] Y.Deng, J.Li. K.H.Shin,T.Viitanen.M.Saeedifard and R.G.Harley," Improved Modulation Scheme for Loss Balancing of Three-Level Active NPC Converters". *IEEE Trans. Power Electron*, vol.32,no.4, pp.2 521-2532., April.2017.

[22] A. K. Gupta and A. M. Khambadkone, "A general space vector PWM algorithm for multilevel inverters, including operation in over modulation range," IEEE Trans. Power Electron., vol. 22, no. 2, pp. 517–526, 2007.

[23] Z.L.Shu, N.Ding,J.Chen, H.F.Zhu and X.Q.He,"Multilevel SVPWM With DC-Link Capacitor Voltage Balancing Control for Diode-Clamped Multilevel Converter Based STATCOM," *IEEE Trans. Ind. Electron.*,vol.60,no.5,pp,1884-1896,May 2013.

[24] A. Mohamed.A.S, A.Gopinath and M.R.Baiju," A Simple Space Vector PWM Generation Scheme for Any General n-Level Inverter," *IEEE Trans. Ind. Electron.*,vol.56,no.5, pp,1649-1656, May,2009.

[25] A. Gupta and A. Khambadkone, "A space vector PWM scheme for multilevel inverters based on two-level space vector PWM," IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1631–1639, Oct. 2006.

[26] Albatran S, Yong Fu, Albana A, "Comprehensive mathematical description and harmonic analysis of hybrid two dimensional three dimensional space vector modulation," *IEEE Trans. Power Electron.*, vol.61,no. 7,pp.3327-3336,Jul. 2014.

[27] M.M Prats, L.G. Franquelo, R.Portillo, J.I.Leon, E.Galvan and J.M. Carrasco," A-3-D Space vector modulation generalized algorithm for multilevel converters", *IEEE Power Electronics Letter*, vol.1, no.4,pp.110-114,Dec, 2003.

[28] M,Zhang, B.Ji, Armstrong M, M.Ma," A near state three dimensional space vector modulation for a three phase four leg voltage source inverter", *IEEE Tran. Power Electron*., vol.29, no.11,pp.5715-5726, Nov.2014.

[29] Y. Deng, K. H. Teo, and R. G. Harley, "Generalized DC-link voltage balancing control method for multilevel inverters," in *Proc. IEEE Appl.Power Electron. Conf. Expo.*, Mar. 2013, pp. 1219–1225.

[30] Y.Deng. R.G.Harley," Space-Vector Versus Nearest-Level Pulse Width Modulation for Multilevel Converters", *IEEE Trans. Power Electron*.,vol30,no.6,pp.2962-2974.June.2015.

[31] A. Ovalle, M..E. Hernandez, G.A. Ramos. A Flexible Nonorthogonal-Reference-Frame-Based SVPWM Framework for Multilevel Inverters", *IEEE Trans. Power Electron*., vol.32, no.6,pp,4925-4938 June 2017.

[32] Y.Deng, K.H.Teo, C.J.Duan, T.G.Habetler and R.G.Harley," A Fast and Generalized Space Vector Modulation Scheme for Multilevel Inverters", *IEEE Trans. Power Electron*., vol.29,No.10, ,pp.5204-5217, 2014.

[33] Y.Deng,Y.Wang, K.H. Teo and R.G.Harley," A Simplified Space Vector Modulation Scheme for Multilevel Converters", *IEEE Trans. Power Electron*., vol.31.no.3,pp.1873-1886.March.2016.

[34] Y. Deng, Y.B.Wang, K.H.Teo. M.Saeedifard, R.G.Harley. Optimized Control of the Modular Multilevel Converter Based on Space Vector Modulation[J]. IEEE Trans on Power Electron. vol. 33, no. 7, pp. 5697–5711, 2018.

[35] K.J.Pratheesh, G.Jagadanand and R.Ramchand," A Generalized -Switch-Matrix-Based Space Vector Modulation Technique Using the Nearest Level Modulation Concept for Neutral-Point-Clamped Multilevel Inverter," *IEEE Trans. Ind. Electron.*,vol.65,no.6, pp,4542-4552, 2018.

[36] L.Zhang, Y.Wang, G.J.Tan, H.Li and Y.F.Zhang," A Novel SVPWM Algorithm for Five-Level Active Neutral-Point-Clamped Converter," IEEE Trans on Power Electron. vol. 31, no. 5, pp. 3859–3865, 2016.